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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/726,860	11/30/2000	Etsuo Morita	09792909-4715	1967

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SONNENSCHN NATH & ROSENTHAL LLP
P.O. BOX 061080
WACKER DRIVE STATION, SEARS TOWER
CHICAGO, IL 60606-1080

EXAMINER

ANDERSON, MATTHEW A

ART UNIT	PAPER NUMBER
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1765

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	09/726,860	MORITA, ETSUO	
	Examiner	Art Unit	
	Matthew A. Anderson	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 July 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-5 and 7-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-5 and 7-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 November 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3-5, 7-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyoku et al. (US 6,153,010) in view of Sugiura (US6,015,979).

Kiyoku et al. discloses methods of growing nitride semiconductors. Figs. 6a-6C show an embodiment of the methods presented. The method is described in col. 13 (lines 25+) and col. 14 lines 1-65. A monocrystalline substrate (11) is overlaid with an underlayer (also known in the art as a buffer layer). The material choices for the substrate are given as sapphire (known chemically as Al_2O_3), spinel (chemically, MgAl_2O_4), SiC of any of the 6H, 4H and 3C polytypes, ZnS, , GaAs, Si, and (although they are less preferred) ZnO or $\text{La}_x\text{Sr}_{1-x}\text{Al}_y\text{Ta}_{1-y}\text{O}_3$. (see col. 7 lines 20-25.) The buffer layer can be AlN, GaN, AlGaN, or InGaN. (col. 13 lines 10-20). The mask is described as being one or a combination of oxides and nitrides such as silicon dioxide (SiO_x), silicon nitride (Si_xN_y), titanium oxide (TiO_x) and zirconium oxide (ZrO_x). Also the metals with melting points greater than 1200°C can be used. These include W, Ir, Pt, Ti etc. Stripe, dots or lattice patterns are disclosed for the mask in col. 8 lines 25-35. In

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col. 14 lines 33-40 it is disclosed that repeated cycles of growth mask formation followed by nitride growth are possible. Polishing the grown nitride is disclosed in col. 13 lines 25-40 to provide a flat growth surface before additional growth iterations are performed. In col. 12 lines 5-15 it is disclosed that the dissimilar substrate (i.e. the basal layer) may be removed from the formed device. The use of a superlattice or graded buffer layer (the first crystal layer) is described in col. 20 lines 20-30 as formed from alternating nitride layers having different compositions.

Kiyoku et al. does not suggest the same method of forming the growth masks as is used in the application.

Sugiura et al. discloses the formation of growth masks for nitride epitaxy as in Fig. 11. This is disclosed in col. 18 lines 9-35 as consisting of a nitride layer on which a SiO_2 layer is formed. This layer is then patterned using a electron beam resist and patterned using a dry etching technique. This suggests etching the underlying nitride layer since the oxide is completely etched through to expose the underlying layer. Also suggested in col. 12 lines 57+, after the mask is patterned, the mask is cleaned with acid. Acid cleaning suggests etching and removal after patterning which exposes the underlying nitride semiconductor.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to combine the references cited because Kiyoku et al. discloses the formation of patterned striped growth masks on a nitride layer and Sugiura et al. discloses an alternative method of forming such masks on a nitride layer. The

motivation for the combination is the increased process flexibility thus afforded and the expectation of better results from the removal of possible contamination from the mask.

In respect to claims 1, 15, it would have been obvious to one of ordinary skill in the art at the time of the present invention to perform III-V nitride compound growth as per the claims including a second growth step through the etched mask and the etched first crystal (i.e. buffer layer), a second etching step to form the second layer through the second pattern, because this was the essence of Kiyoku's Figs. Figs. 1A-1C and 6A-6C with the above modification of Sugiura et al.

Further in respect to claims 1 and 15, it would have been obvious to one of ordinary skill in the art at the time of the present invention that the etching steps include etching the crystal layers through the mask because such removal and acid cleaning of parts of the mask pattern is described by Sugiura et al. Sugiura et al. suggests (col. 12 lines 57+) the acid cleaning (i.e etching) of the mask before growth of a nitride through the openings in it.

In respect to claim 3, it would have been obvious to one of ordinary skill in the art at the time of the present invention that the mask pattern include an underlayer and an upper layer because Kiyoku et al. discloses multi-layer growth masks.

In respect to claim 4, it would have been obvious to one of ordinary skill in the art at the time of the present invention to form the mask from different materials having different properties (such as SiO_2 and Si_3N_4) because such is explicitly disclosed by Kiyoku et al.

In respect to claim 5, it would have been obvious to one of ordinary skill in the art at the time of the present invention that the windows of the first mask and the second mask do not overlie one another in the direction of the thickness of the crystal because such mask overlay is shown in Fig. 6A-6C of Kiyoku et al.

In respect to claims 7 and 16, it would have been obvious to one of ordinary skill in the art at the time of the present invention to remove the basal layer after the growth of the device layers of nitride is completed because such is suggested by Kiyoku et al.

In respect to claims 8 and 9, it would have been obvious to one of ordinary skill in the art at the time of the present invention to form a buffer layer (i.e. an inner layer) of differently composed III-V nitride layers because such is suggested by Kiyoku et al. in such an epitaxial process.

In respect to claims 10 and 11, it would have been obvious to one of ordinary skill in the art at the time of the present invention to form the first mask layer in stripes arranged in one direction in a plane almost parallel to the surface of the basal plane because Kiyoku et al. discloses flattening the layer before subsequent growth and such planarization would have been anticipated those of ordinary skill in the art to produce a better surface.

In respect to claim 12, it would have been obvious to one of ordinary skill in the art at the time of the present invention that the first and second mask pattern include elements arranged in two directions in a plane almost parallel to the surface of the basal body (i.e. in a lattice pattern) because such is explicitly suggested by Kiyoku et al.

In respect to claim 13, it would have been obvious to one of ordinary skill in the art at the time of the present invention to use silicon oxide or silicon nitride masking materials because such were explicitly suggested by Kiyoku et al.

In respect to claim 14, it would have been obvious to one of ordinary skill in the art at the time of the present invention to use a substrate (i.e. basal body) of sapphire, or SiC or GaAs etc. because such is disclosed by Kiyoku et al.

In respect to claims 17-22, it would have been obvious to one of ordinary skill in the art at the time of the present invention to repeat the steps of the nitride growth to grow a third crystal layer from the second crystal layer because Kiyoku et al. suggests such iterations in col. 14 lines 33-40.

Response to Arguments

3. Applicant's arguments filed 7/26/2004 have been fully considered but they are not persuasive.

The argument that Kiyoku et al. teaches away from etching the crystal layers through the mask patterns is not convincing. The rejection is based on a combination of references which together suggest the acid cleaning of the patterned mask before crystal growth through that mask. Since the mask is patterned, one of ordinary skill in the art would expect the acid cleaning agent to contact the crystal layer and thus etch it.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew A. Anderson whose telephone number is (571) 272-1459. The examiner can normally be reached on M-F, 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571) 272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MAA

January 4, 2005

NADINE G. NORTON
SUPERVISORY PATENT EXAMINER
